FIG. 1

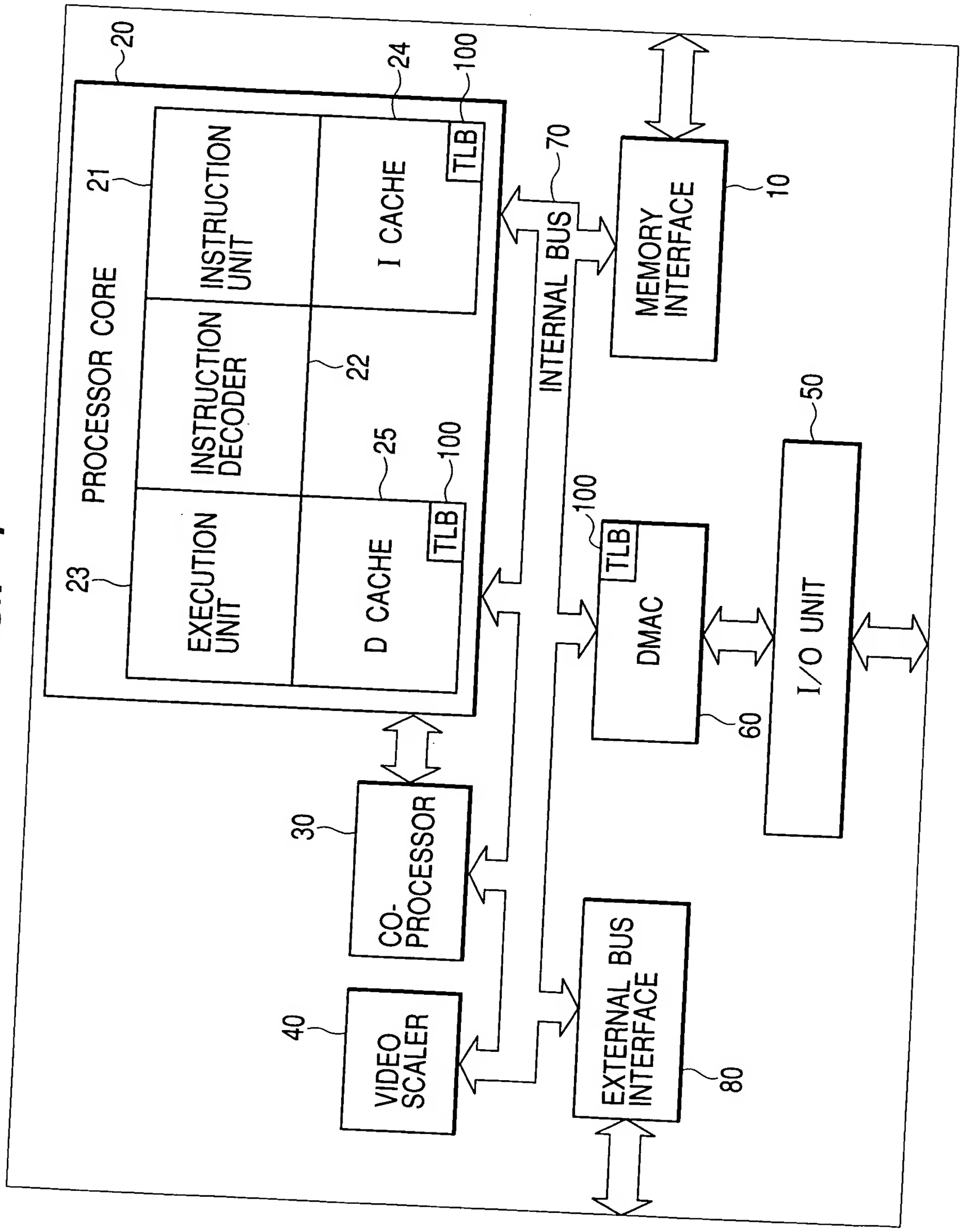

20
24
100
21
INSTRUCTION UNIT
I CACHE
TLB
PROCESSOR CORE
INSTRUCTION DECODER
22
23
EXECUTION UNIT
D CACHE
25
TLB
70
EXTERNAL BUS
MEMORY INTERFACE
10
100
TLB
DMAC
60
50
I/O UNIT
30
CO-PROCESSOR
40
VIDEO SCALER
EXTERNAL BUS INTERFACE
80

FIG. 2

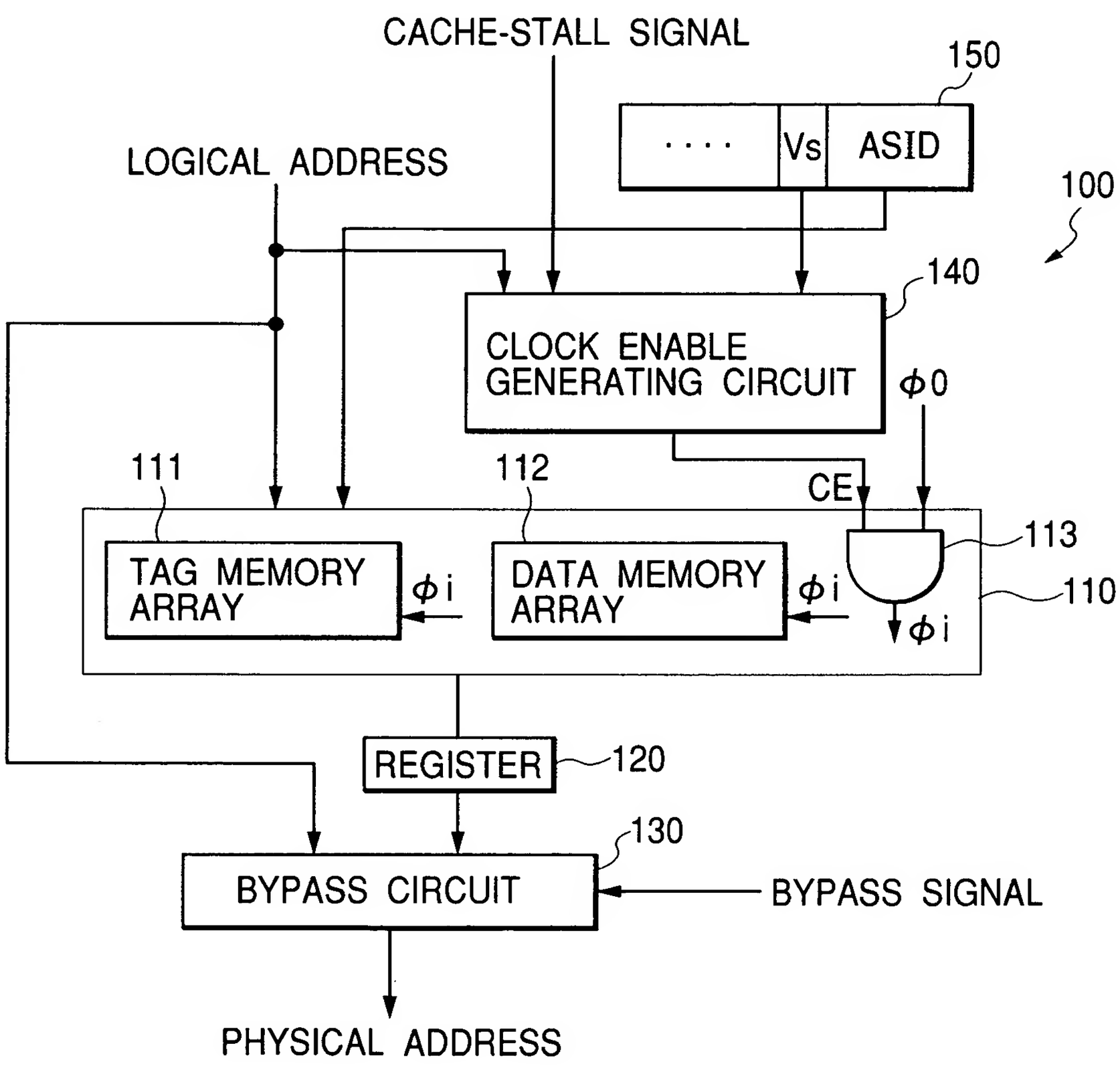

CACHE-STALL SIGNAL
150
· · · ·
Vs
ASID
LOGICAL ADDRESS
100
140
CLOCK ENABLE GENERATING CIRCUIT
φ0
111
112
CE
113
TAG MEMORY ARRAY
φi
DATA MEMORY ARRAY
φi
110
φi
REGISTER
120
130
BYPASS CIRCUIT
BYPASS SIGNAL
PHYSICAL ADDRESS

FIG. 3

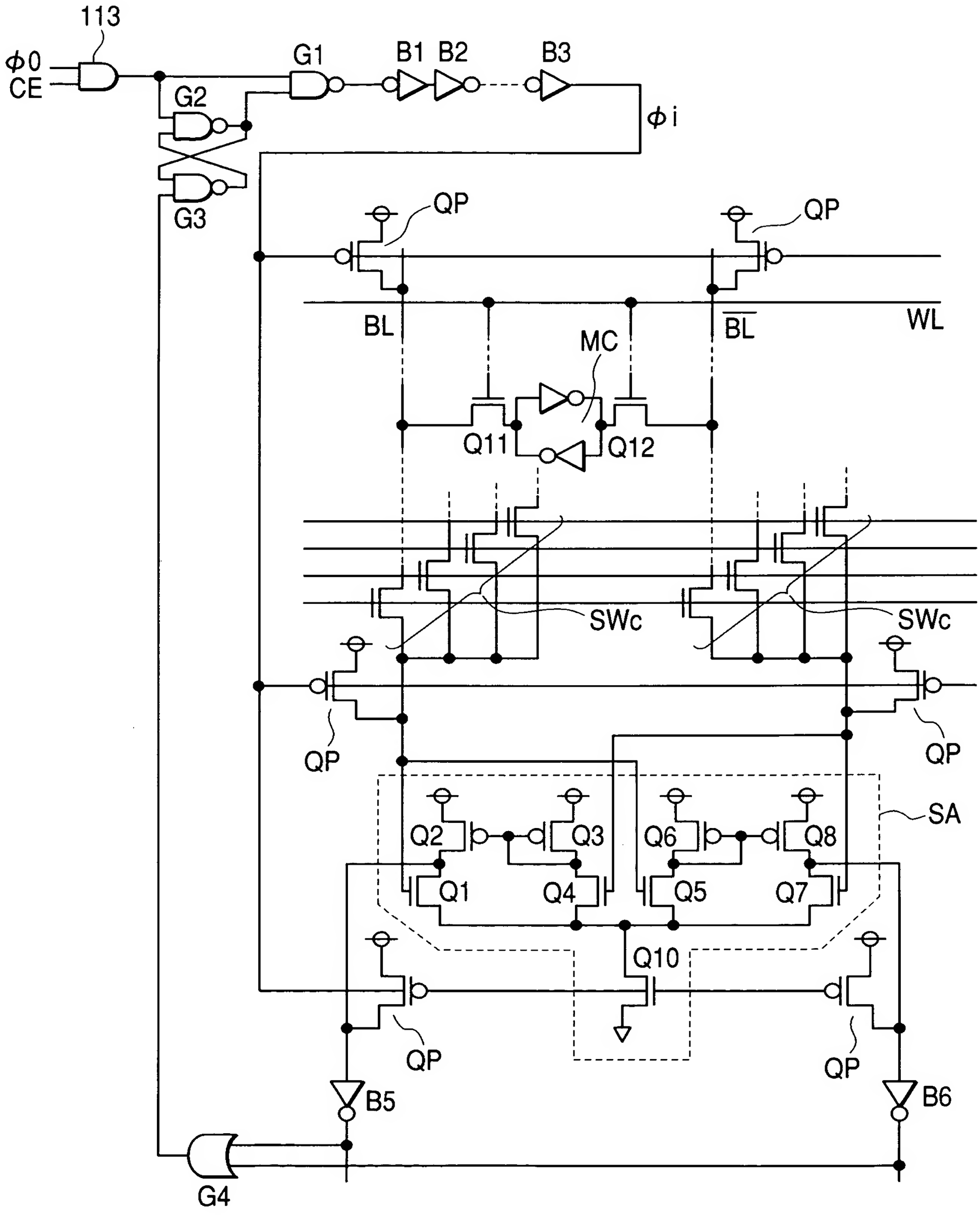

113
φ0
CE
G1
B1
B2
B3
φi
G2
G3
QP
QP
BL
BL
WL
MC
Q11
Q12
SWc
SWc
QP
QP
QP
QP
SA
Q2
Q3
Q6
Q8
Q1
Q4
Q5
Q7
Q10
B5
B6
G4

FIG. 4

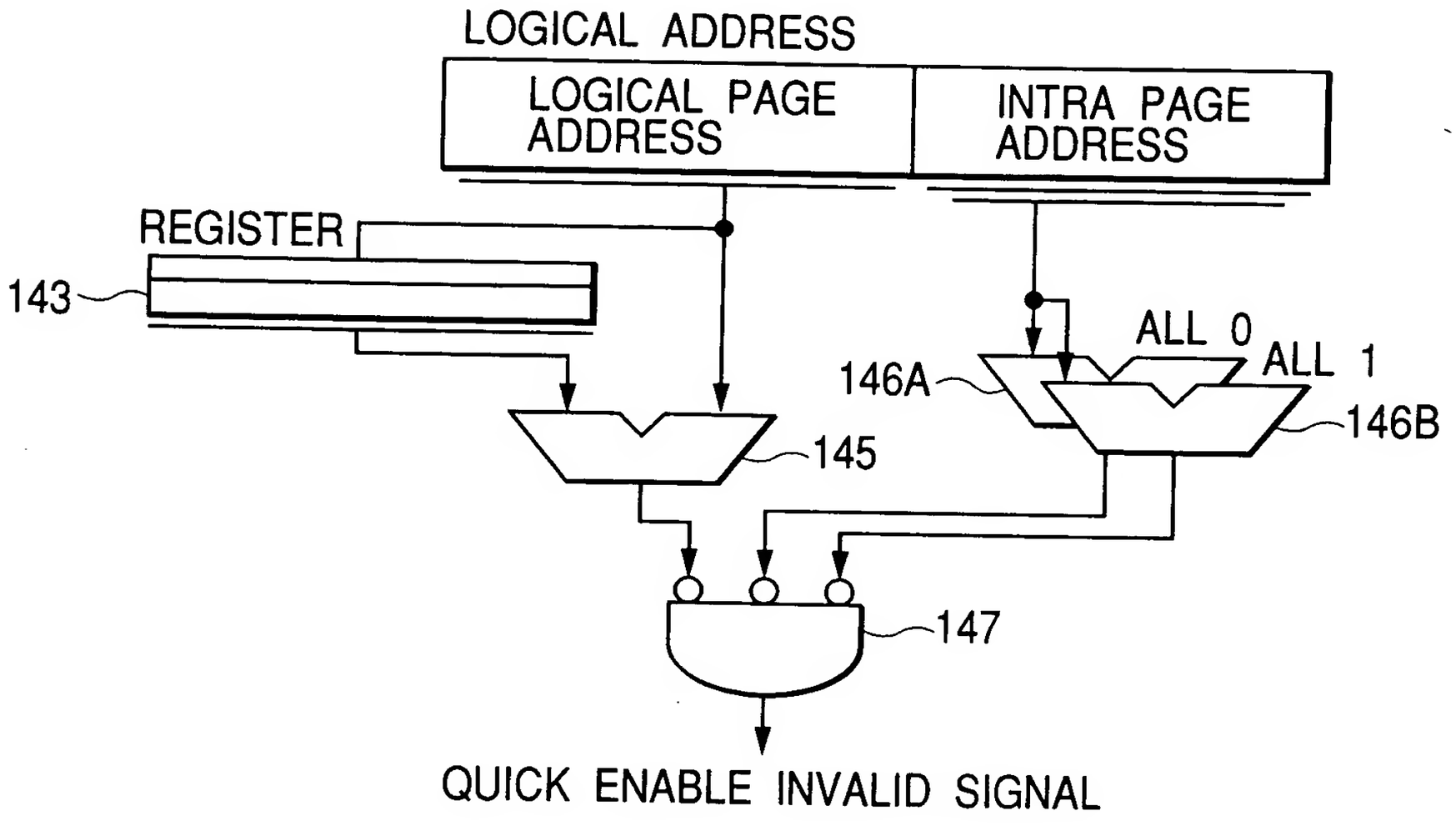

LOGICAL ADDRESS
LOGICAL PAGE ADDRESS
INTRA PAGE ADDRESS
REGISTER
143
ALL 0
ALL 1
146A
146B
145
147
QUICK ENABLE INVALID SIGNAL

FIG. 5(a)

V-BIT IS 0 IN THE STATUS REGISTER

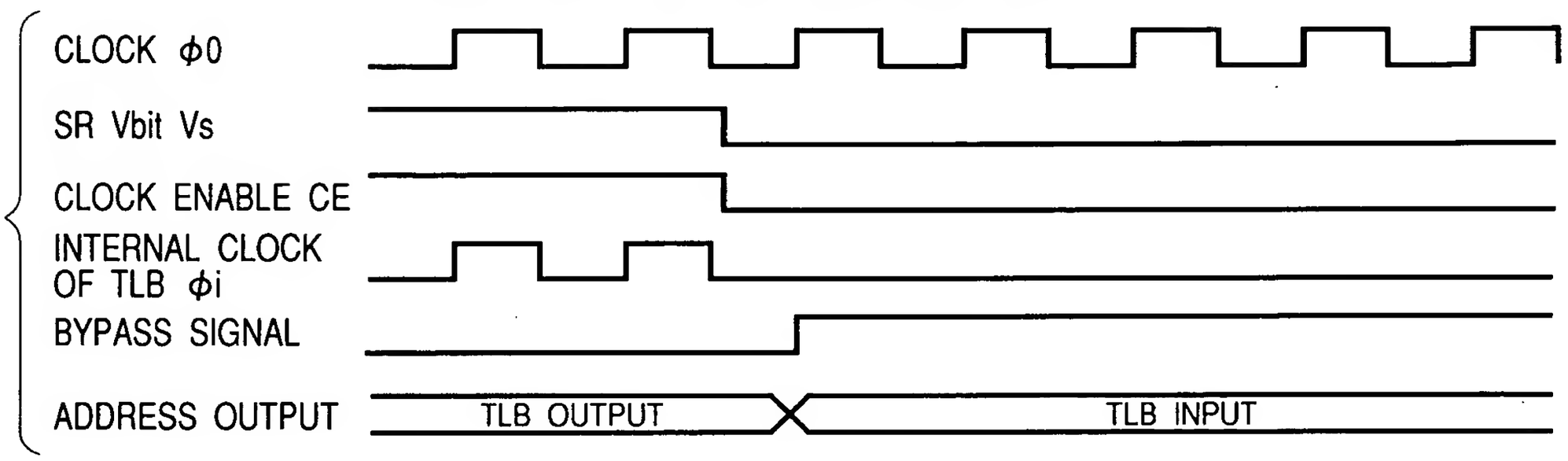


FIG. 5(b)

CACHE-STALL SIGNAL IS HIGH LEVEL

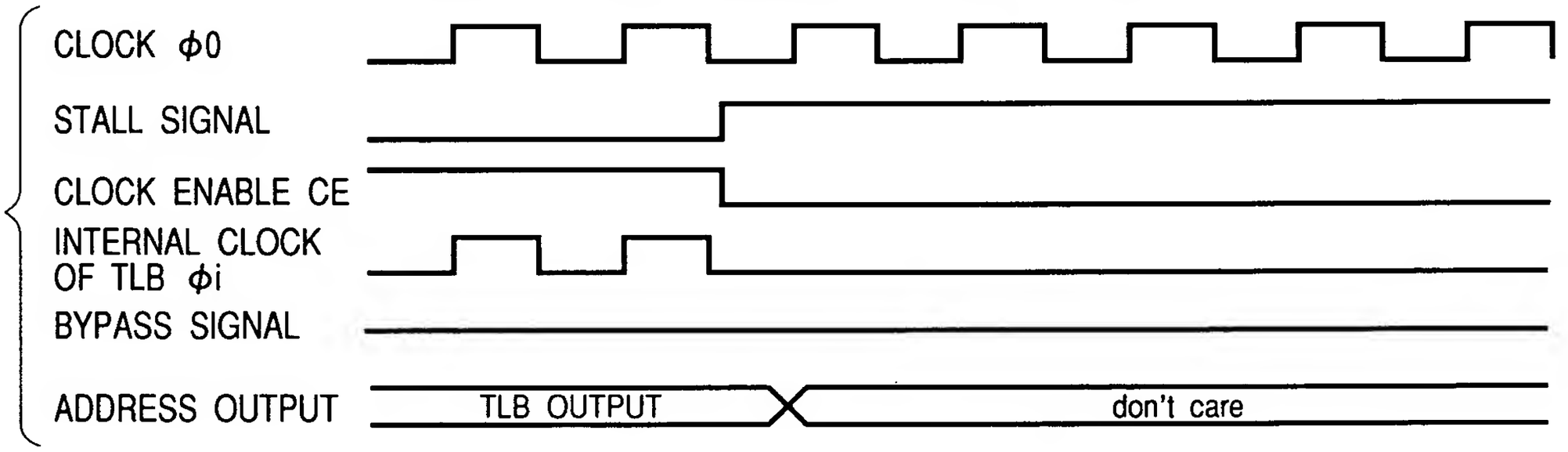


FIG. 5(c)

SAME PAGE ADDRESS IS ACCESSED

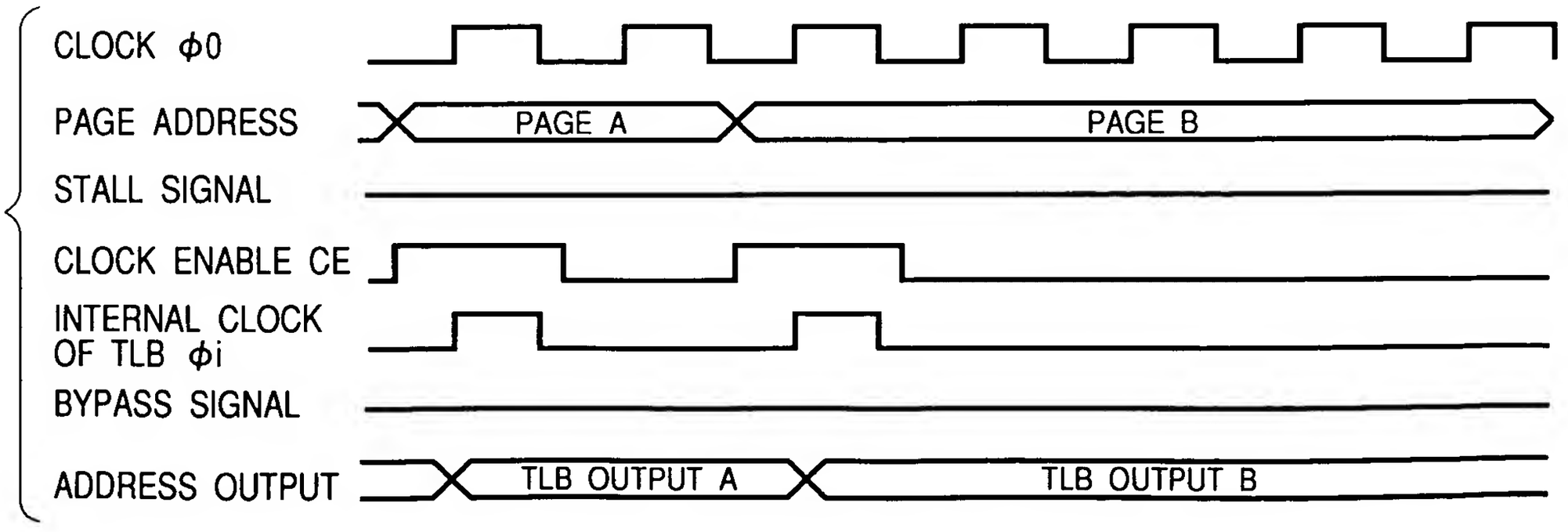


FIG. 6

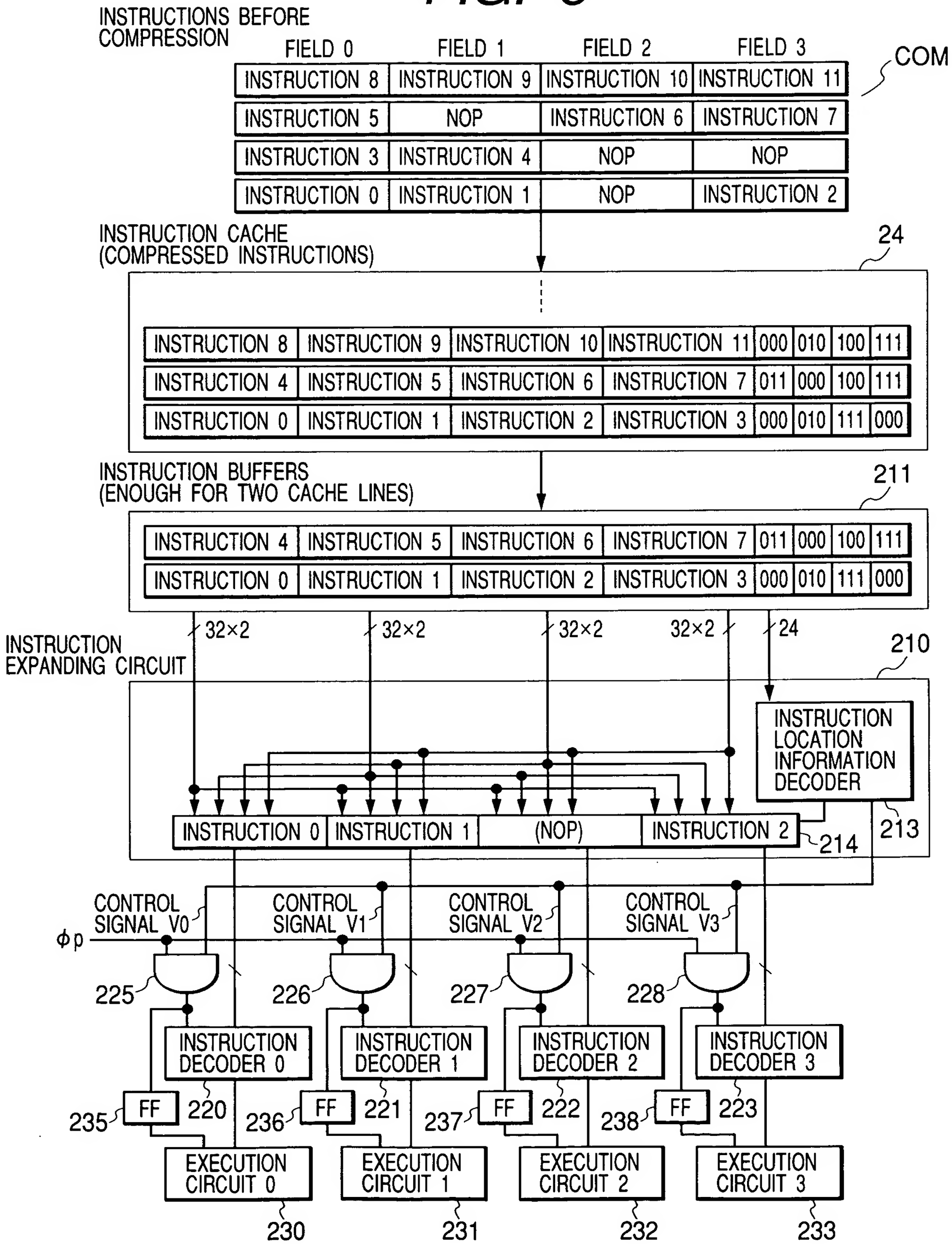

INSTRUCTIONS BEFORE COMPRESSION
FIELD 0
FIELD 1
FIELD 2
FIELD 3
COM
INSTRUCTION 8
INSTRUCTION 9
INSTRUCTION 10
INSTRUCTION 11
INSTRUCTION 5
NOP
INSTRUCTION 6
INSTRUCTION 7
INSTRUCTION 3
INSTRUCTION 4
NOP
NOP
INSTRUCTION 0
INSTRUCTION 1
NOP
INSTRUCTION 2
INSTRUCTION CACHE (COMPRESSED INSTRUCTIONS)
24
INSTRUCTION 8
INSTRUCTION 9
INSTRUCTION 10
INSTRUCTION 11
000
010
100
111
INSTRUCTION 4
INSTRUCTION 5
INSTRUCTION 6
INSTRUCTION 7
011
000
100
111
INSTRUCTION 0
INSTRUCTION 1
INSTRUCTION 2
INSTRUCTION 3
000
010
111
000
INSTRUCTION BUFFERS (ENOUGH FOR TWO CACHE LINES)
211
INSTRUCTION 4
INSTRUCTION 5
INSTRUCTION 6
INSTRUCTION 7
011
000
100
111
INSTRUCTION 0
INSTRUCTION 1
INSTRUCTION 2
INSTRUCTION 3
000
010
111
000
32×2
32×2
32×2
32×2
24
INSTRUCTION EXPANDING CIRCUIT
210
INSTRUCTION LOCATION INFORMATION DECODER
213
INSTRUCTION 0
INSTRUCTION 1
(NOP)
INSTRUCTION 2
214
CONTROL SIGNAL V0
CONTROL SIGNAL V1
CONTROL SIGNAL V2
CONTROL SIGNAL V3
φp
225
226
227
228
INSTRUCTION DECODER 0
INSTRUCTION DECODER 1
INSTRUCTION DECODER 2
INSTRUCTION DECODER 3
235
FF
220
236
FF
221
237
FF
222
238
FF
223
EXECUTION CIRCUIT 0
EXECUTION CIRCUIT 1
EXECUTION CIRCUIT 2
EXECUTION CIRCUIT 3
230
231
232
233

FIG. 7

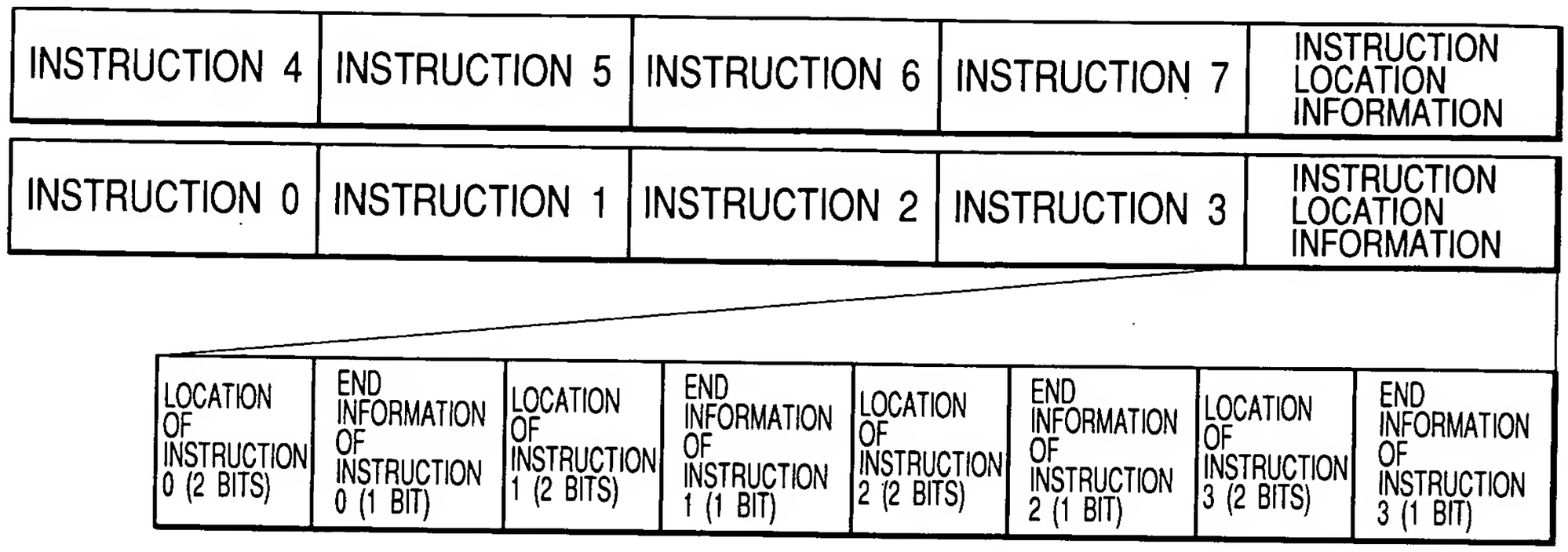


FIG. 8

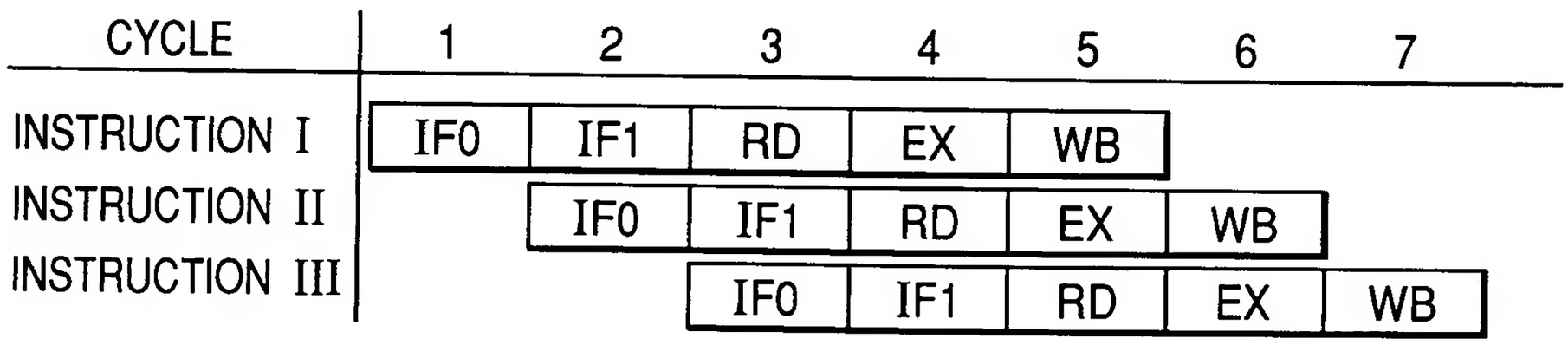
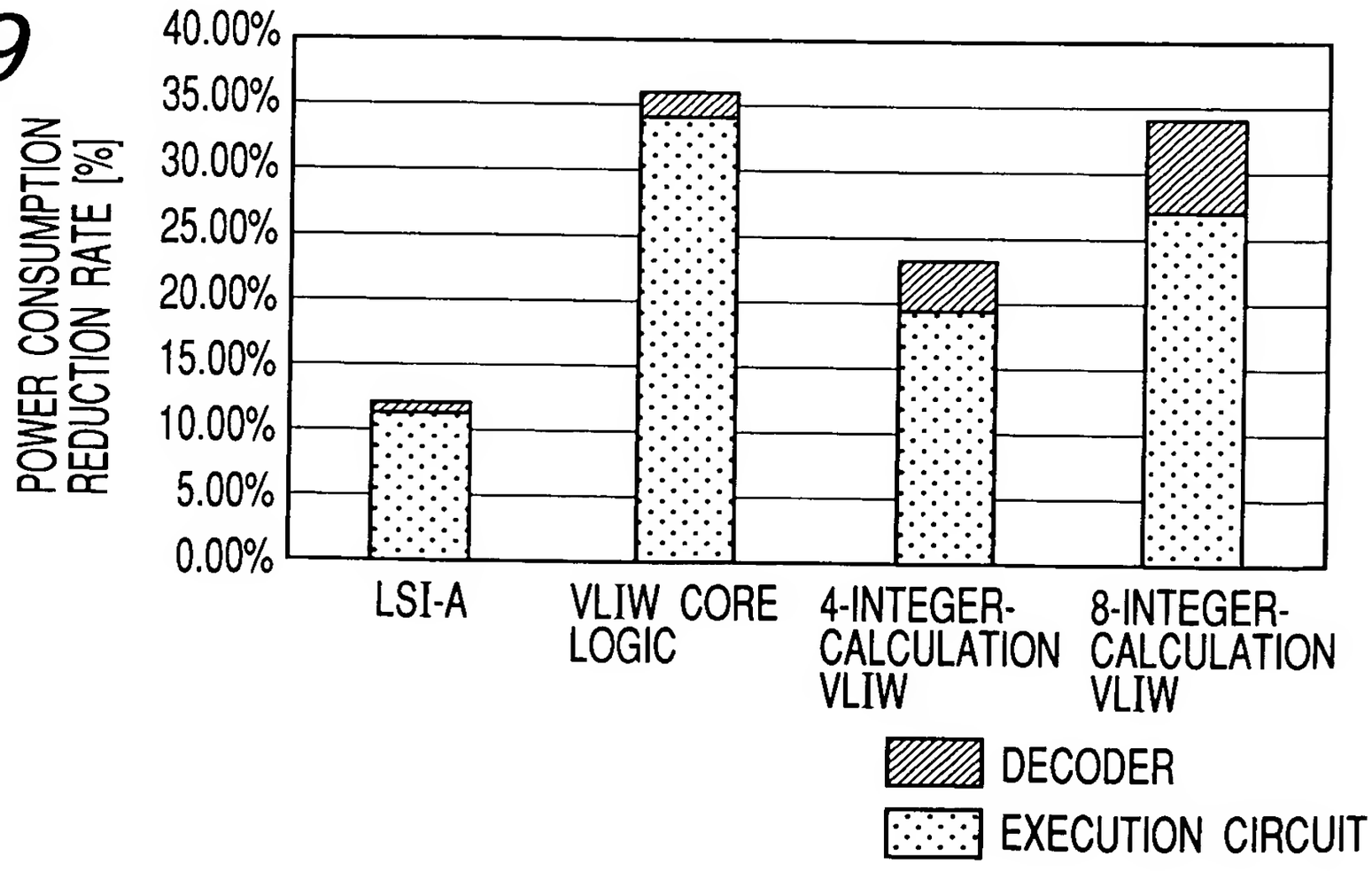


FIG. 9



8 / 8

FIG. 10(a)

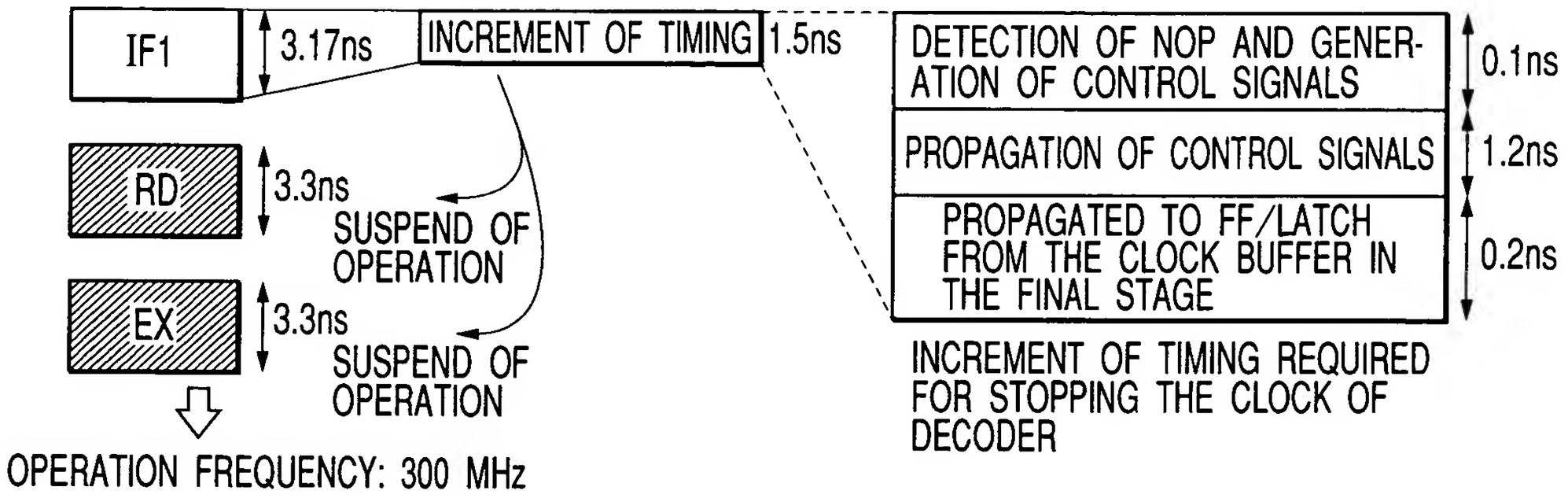


FIG. 10(b)